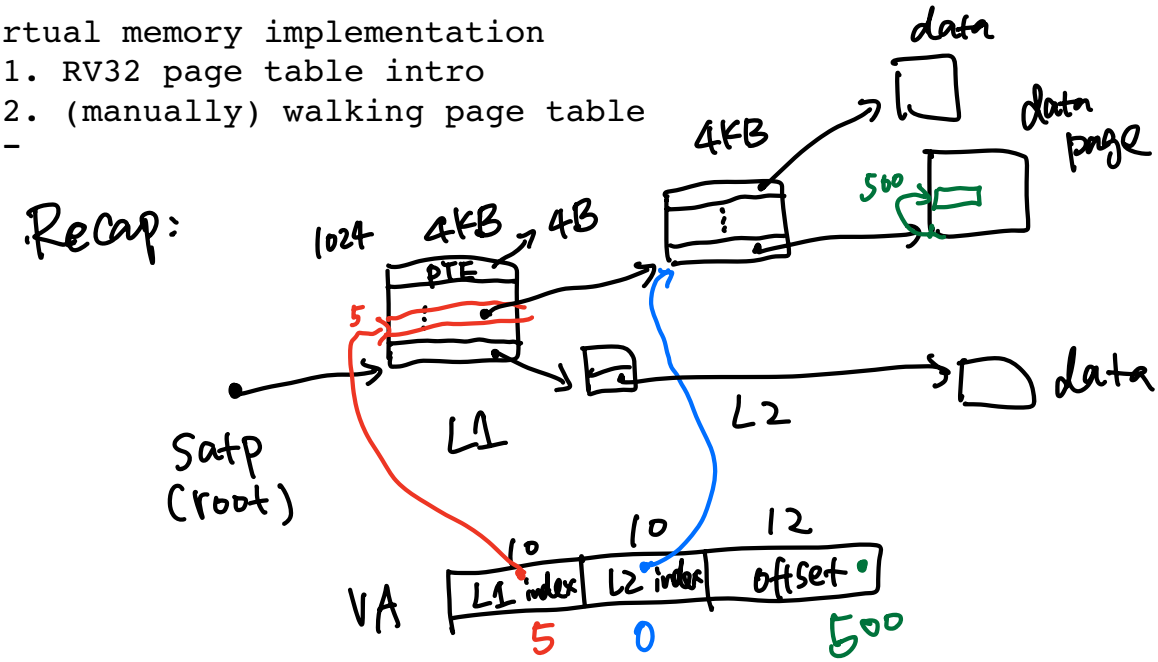
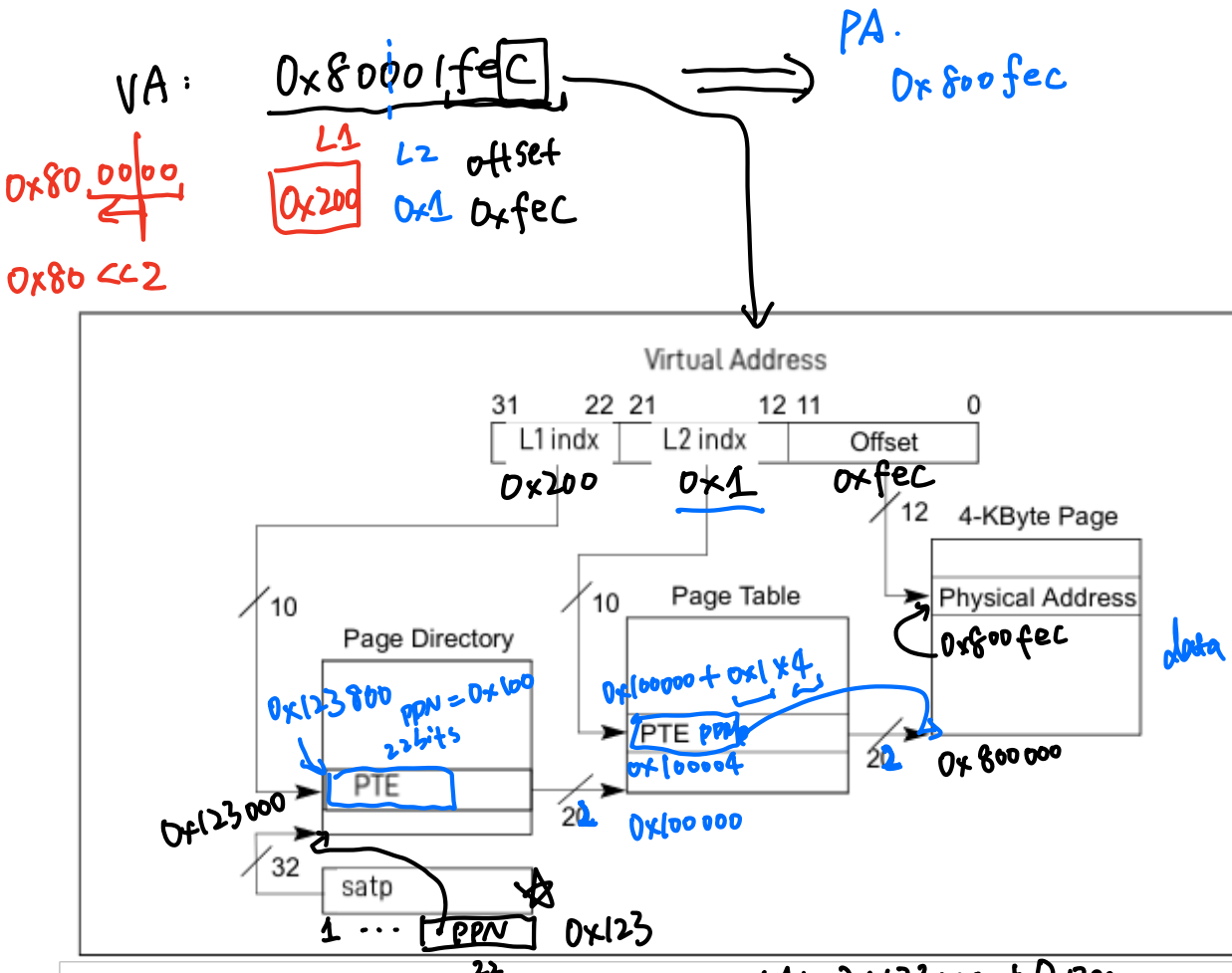
Virtual memory implementation
☐ 1. RV32 page table intro
☐ 2. (manually) walking page table





OSI Week8

4. CSR satp (page table root)

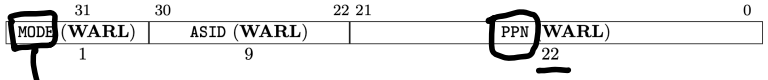


Figure 4.14: Supervisor address translation and protection register **satp** when SXLEN=32.

(1-bit MODE)

SXLEN=32		
Value	Name	Description
0	Bare	No translation or protection.
1	Sv32	Page-based 32-bit virtual addressing (see Section 4.3).

physical memory size:
$= 2^{22} \cdot 4KB$
$= 16GB.$

2. Page table entry (PTE)

22 PPN

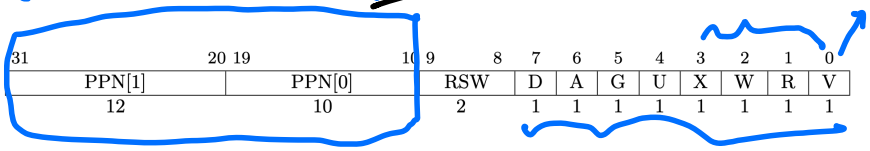


Figure 4.18: Sv32 page table entry.

3. Virtual address (VA)

VPN
20bits

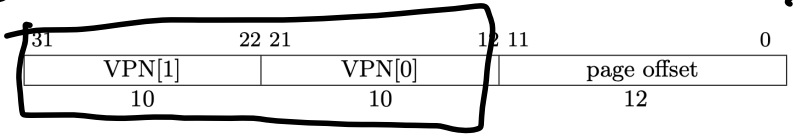


Figure 4.16: Sv32 virtual address.

Virtual memory size
$= 2^{20} \cdot 4KB$
$= 4GB$

Simulate CPU: manual page walk

Steps:
 (1) split the VA to l1/l2 indexes and offest
 (2) get the root of page table
 (3) calc the L1 page
 (4) calc the L2 page
 (5) calc the physical address