3.7.2.2 Using SDMA

The sequence for using SDMA is shown below.
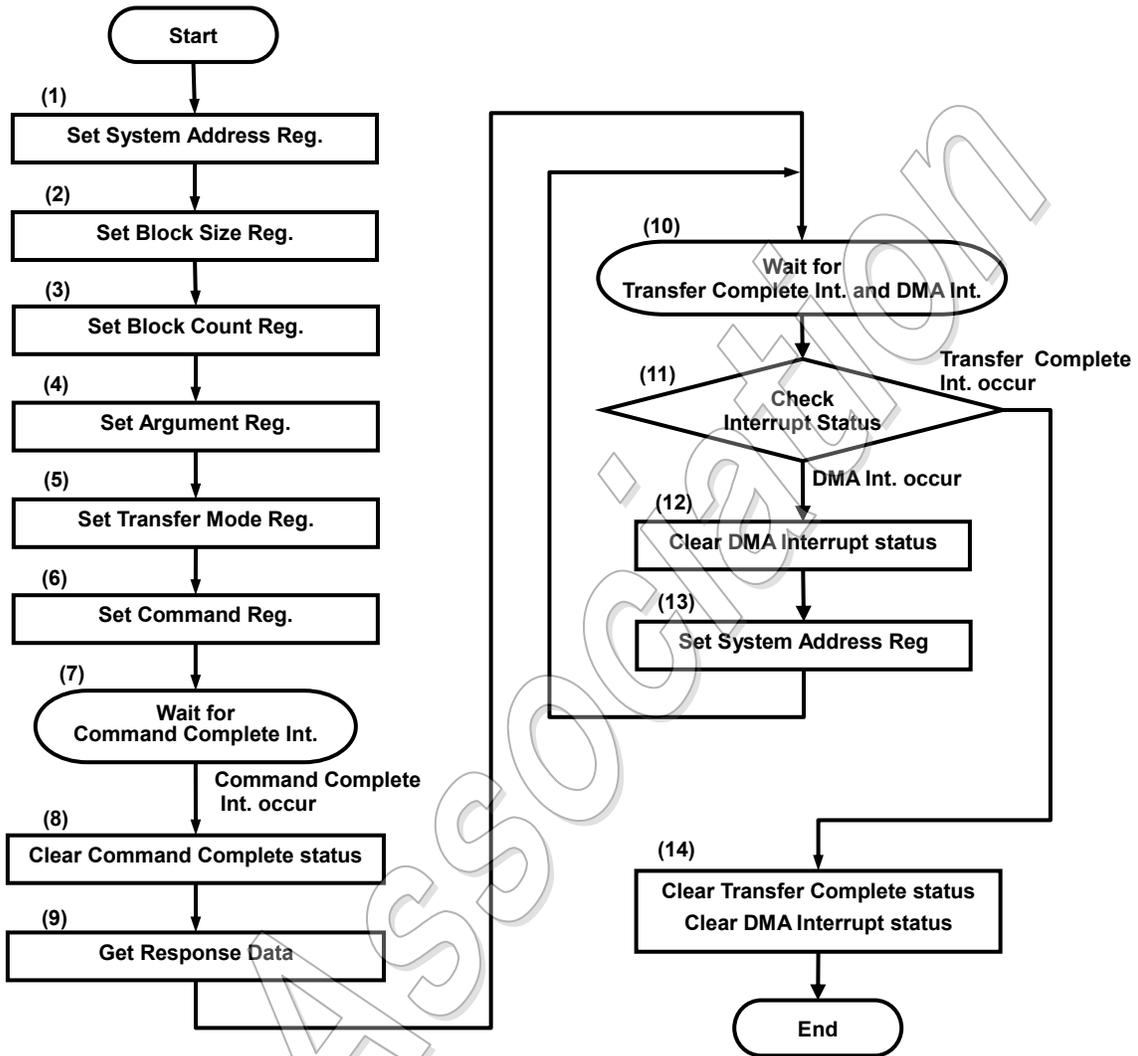

Figure 3-14: Transaction Control with Data Transfer Using DAT Line Sequence (Using SDMA)

(1) Data location of system memory is set to the *SDMA System Address* register ~~if **Host Version 4 Enable =** 0 or set to *ADMA System Address* register if **Host Version 4 Enable = 1**~~.

(2) Set the value corresponding to the executed data byte length of one block in the *Block Size* register.

(3) Set the value corresponding to the executed data block count in the *Block Count* register in accordance with Table 2-9. Refer to Section 1.15 for more details.

(4) Set the argument value to the *Argument* register.

(5) Set the value to the *Transfer Mode* register. The Host Driver determines **Multi / Single Block Select, Block Count Enable**, **Data Transfer Direction**, **Auto CMD12 Enable** and **DMA Enable**. **Multi / Single Block Select** and **Block Count Enable** are determined according to Table 2-9.
~~If response check is enabled (Response Error Check Enable =1), set Response Interrupt Disable to 1 and select Response Type R1 / R5.~~

(6) Set the value to the *Command* register.
Note: When writing to the upper byte [3] of the *Command* register, the SD command is issued and SDMA is started.

(7) ~~If response check is enabled, go to stop (10) else~~ wait for the **Command Complete** Interrupt.

(8) Write 1 to the **Command Complete** in the *Normal Interrupt Status* register to clear this bit.

(9) Read *Response* register and get necessary information of the issued command.

(10) Wait for the **Transfer Complete** Interrupt and **DMA Interrupt**.

(11) If **Transfer Complete** is set to 1, go to Step (14) else if **DMA Interrupt** is set to 1, go to Step (12).**Transfer Complete** is higher priority than **DMA Interrupt**.

(12) Write 1 to the **DMA Interrupt** in the *Normal Interrupt Status* register to clear this bit.

(13) Set the next system address of the next data position to the *System Address* register and go to Step (10).

(14) Write 1 to the **Transfer Complete** and **DMA Interrupt** in the *Normal Interrupt Status* register to clear this bit.

Note: Step (2) and Step (3) can be executed simultaneously. Step (5) and Step (6) can also be executed simultaneously.