2.2.9 Present State Register (Cat.C Offset 024h)

The Host Driver can get status of the Host Controller from this 32-bit read only register.

D31	D30	D29	D28	D27	D26	D25	D24	D23 D20	D19	D18	D17	D16
UHS-II IF Detection	Lane Synchronization	In Dormant State	Sub Command Status	Command Not Issued by Error	Rsvd	Host Regulator Voltage Stable	CMD Line Signal Level	DAT[3:0] Line Signal Level	Write Protect Switch Pin Level	Card Detect Pin Level	Card State Stable	Card Inserted
D15 D12	D11	D10	D09	D08	D07 D04	D03	D02	D01	D00			
Rsvd	Buffer Read Enable	Buffer Write Enable	Read Transfer Active	Write Transfer Active	DAT[7:4] Line Signal Level	Re-Tuning Request	DAT Line Active	Command Inhibit (DAT)	Command Inhibit (CMD)			

Figure 2-9 : Present State Register

Location	Attrib	Register Field Explanation
31	RO	**UHS-II IF Detection (UHS-II Only)** This status indicates whether a card supports UHS-II IF. This status is enabled by setting **UHS-II Interface Enable** to 1 in the *Host Control 2* register. UHS-II interface initialization is activated by setting **SD Clock Enable** in the *Clock Control* register. Host Controller drives STB.L on D0 lane from EIDL state and waits for receiving STB.L on D1 lane. This bit is set to 1 if STB.L is detected on D1 lane. Host Controller shall compensate latency from setting **SD Clock Enable** to output STB.L on D0 lane when reading this status (Refer to Figure 3-36 about details of this method). This bit may be read any time after setting **SD Clock Enable** for faster UHS-II IF detection but Host Driver shall check this status at least 200us period from setting **SD Clock Enable** until detecting UHS-II IF. After UHS-II IF is detected, this bit is cleared by when EIDL is detected on D0 lane, **UHS-II Interface Enable** is set to 0 or Host full reset is executed. 1 – UHS-II IF is detected 0 – UHS-II IF is not detected Refer to Section 3.13.2 for more details about sequence of detecting UHS-II IF and checking PHY Initialization Completion.

<table>
<tr><td></td><td></td><td>(2) When writing a 1 to Continue Request in the Block Gap Control register to restart a read transfer.
This bit shall be cleared in either of the following cases:
(1) When the end bit of the last data block is sent from the SD Bus to the Host Controller. In case of ADMA2, the last block is designated by the last transfer of Descriptor Table.
(2) When a read transfer is stopped at the block gap initiated by a Stop At Block Gap Request.

The Host Controller shall stop read operation at the start of the interrupt cycle of the next block gap by driving Read Wait or stopping SD clock. If the Read Wait signal is already driven (due to data buffer cannot receive data), the Host Controller can continue to stop read operation by driving the Read Wait signal. It is necessary to support Read Wait in order to use Suspend/Resume function.

(b) In the case of write transactions
This status indicates that a write transfer is executing on the SD Bus. Changing this value from 1 to 0 generate a Transfer Complete interrupt in the Normal Interrupt Status register. Refer to Section 3.12.4 for sequence details.

This bit shall be set in either of the following cases:
(1) After the end bit of the write command.
(2) When writing to 1 to Continue Request in the Block Gap Control register to continue a write transfer.
This bit shall be cleared in either of the following cases:
(1) When the SD card releases write busy of the last data block. If SD card does not drive busy signal for 8 SD Clocks, the Host Controller shall consider the card drive "Not Busy". In case of ADMA2, the last block is designated by the last transfer of Descriptor Table.
(2) When the SD card releases write busy prior to waiting for write transfer as a result of a Stop At Block Gap Request.

(c) Command pairing with response-with-busy
This status indicates whether a command indicates busy (e.g., erase command for memory) is executing on the SD Bus. This bit is set after the end bit of the command and is cleared when busy after the response is de-asserted. Changing this bit from 1 to 0 generate a Transfer Complete interrupt in the Normal Interrupt Status register. Refer Figure 2-11 to Figure 2-13.

<table>
<tr><td>1</td><td>DAT Line Active</td></tr>
<tr><td>0</td><td>DAT Line Inactive</td></tr>
</table>
</td></tr>
<tr><td>01</td><td>ROC</td><td>Command Inhibit (DAT) (SD Mode only)
Setting this status to 1 indicates that Host Controller is currently in a state, which cannot issue a command using DAT line. While data transfer is being stopped by Stop At Block Gap Request, Host Driver shall not issue any command using DAT line (except an abort command) regardless of this status.
This status bit is generated if either the DAT Line Active or the Read Transfer Active is set to 1. If this bit is 0, it indicates the Host Controller can issue the next SD Command. Commands with busy signal belong to Command Inhibit (DAT) (ex. R1b, R5b type). Changing from 1 to 0 generates a Transfer Complete interrupt in the Normal Interrupt Status register.
Note: The SD Host Driver can save registers in the range of 000-00Dh for a</td></tr>
</table>

<table>
<tr><td></td><td></td><td>suspend transaction after this bit has changed from 1 to 0.

<table><tr><td>1</td><td>Cannot issue command which uses the DAT line</td></tr><tr><td>0</td><td>Can issue command which uses the DAT line</td></tr></table></td></tr>
<tr><td>00</td><td>ROC</td><td>Command Inhibit (CMD)
Setting this status to 1 indicates that Host Controller is currently in a state, which cannot issue a command using only CMD line or a UHS-II command. While data transfer is being stopped by Stop At Block Gap Request, this status is indicated to 0.
(1) SD Mode
If this bit is 0, it indicates the CMD line is not in use and the Host Controller can issue an SD Command using the CMD line.
This bit is set immediately after the Command register (00Fh) is written. This bit is cleared when the command response is received. Auto CMD12 and Auto CMD23 consist of two responses. In this case, this bit is not cleared by the response of CMD12 or CMD23 but cleared by the response of a read/write command.
Status issuing Auto CMD12 is not read from this bit. Therefore, if a command is issued during Auto CMD12 operation, Host Controller shall manage to issue two commands: CMD12 and a command set by Command register.

Even if the Command Inhibit (DAT) is set to 1, commands using only the CMD line can be issued if this bit is 0. Changing from 1 to 0 generates a Command Complete Interrupt in the Normal Interrupt Status register.
If the Host Controller cannot issue the command because of a command conflict error (Refer to Command CRC Error in Section 2.2.19) or because of Command Not Issued By Auto CMD12 Error (Refer to Section 2.2.24), this bit shall remain 1 and the Command Complete is not set.

(2) UHS-II Mode
This bit is 0 means that a command packet can be issued by the Host Controller. While this bit is set to 1, which means the Host Controller is not ready to issue a next command, Host Driver shall not write the registers from UHS-II Block Size (Offset 080h) to the UHS-II Command (Offset 09Eh). Changing from 1 to 0 generates a Command Complete Interrupt in the Normal Interrupt Status register.

<table><tr><td>1</td><td>Host Controller is not ready to issue a command</td></tr><tr><td>0</td><td>Host Controller is ready to issue a command</td></tr></table>
Version 4.10 adds a new control to prevent error statuses from overwriting by receipt of a next command. This status keeps indicating 1 while any of response error statuses is set to 1 (as described in Section 1.17), Command Not Issued by Error in this register is set to 1 or Command Not Issued by Auto CMD12 Error in the Auto CMD Error Status register is set to 1. Software Reset For CMD Line is used to clear the error statuses above and this status.</td></tr>
</table>

Table 2-16 : Present State Register (Part 2)

Implementation Note:
The Host Driver can issue CMD0, CMD12, CMD13 (for memory) and CMD52 (for SDIO) when the **DAT** lines are busy during data transfer. These commands can be issued when **Command Inhibit (CMD)** is set to zero. Other commands shall be issued when **Command Inhibit (DAT)** is set to zero.

Possible changes to the Physical Layer Specification may add other commands to this list in the future.

Implementation Note:
Some fields defined in the Present State register change values asynchronous to the system clock. The System reads these statuses through the System Bus Interface and it may require data stable period during bus cycle. The Host Controller should sample and hold values during reads from this register according to the timing required by the System Bus Interface specification.

Figure 2-11Figure 2-11 to Figure 2-13 shows the timing of setting and clearing the **Command Inhibit (DAT)** and the **Command Inhibit (CMD)**.

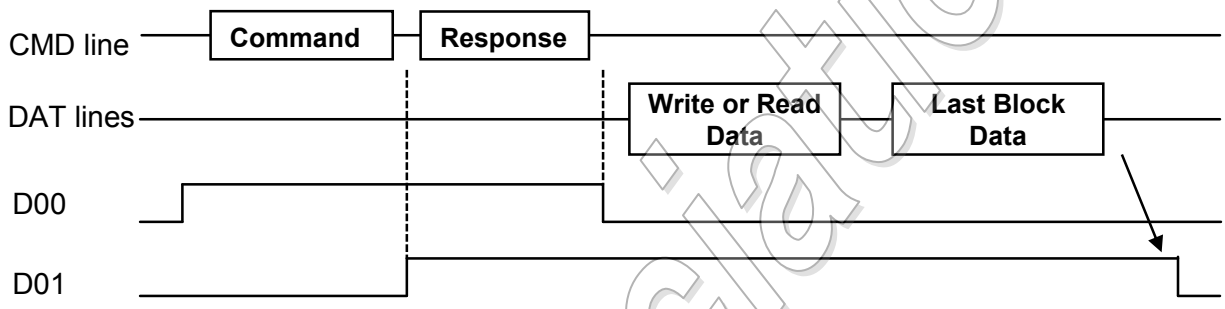

Figure 2-11 : Timing of Command Inhibit (DAT) and Command Inhibit (CMD) with Data Transfer

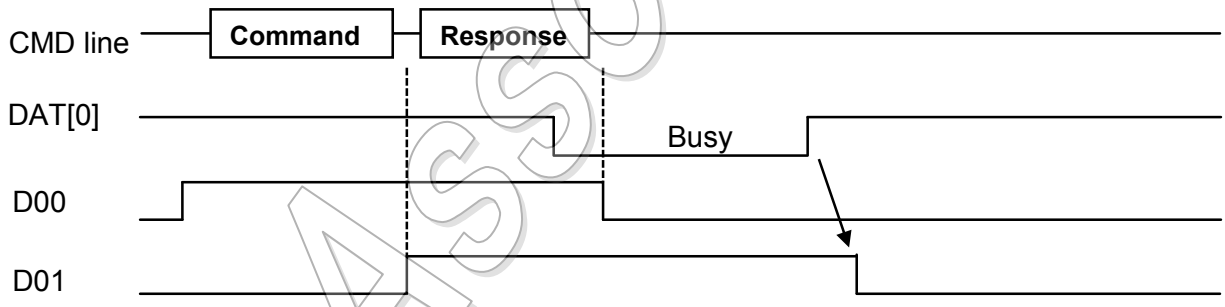

Figure 2-12 : Timing of Command Inhibit (DAT) for the Case of Response with Busy

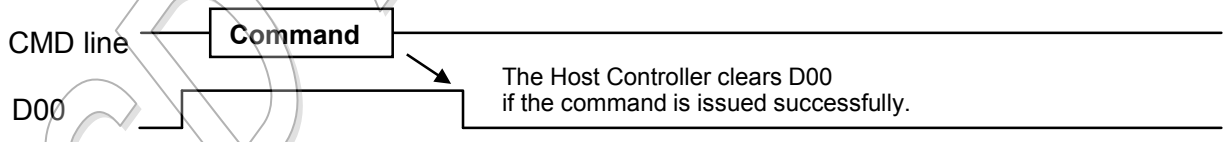

Figure 2-13 : Timing of Command Inhibit (CMD) for the Case of No Response Command

2.2.18 Normal Interrupt Status Register (Cat.C Offset 030h)

The *Normal Interrupt Status Enable* affects reads of this register, but *Normal Interrupt Signal Enable* does not affect these reads. An interrupt is generated when the Normal Interrupt Signal Enable is enabled and at least one of the status bits is set to 1. Writing 1 to a bit of RW1C attribute clears it; writing 0 keeps the bit unchanged. Writing 1 to a bit of ROC attribute keeps the bit unchanged. More than one status can be cleared with a single register write. The **Card Interrupt** is cleared when the card stops asserting the interrupt; that is, when the Card Driver services the interrupt condition.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Error Interrupt	Rsvd	FX Event	Re-Tuning Event	INT_C	INT_B	INT_A	Card Interrupt	Card Removal	Card Insertion	Buffer Read Ready	Buffer Write Ready	DMA Interrupt	Block Gap Event	Transfer Complete	Command Complete

Figure 2-21 : Normal Interrupt Status Register

Location	Attrib	Register Field Explanation
15	ROC	**Error Interrupt** This status is set to 1 when any of the bits is set in the *Error Interrupt Status* register and in the *UHS-II Error Interrupt Status* register so that the Host Driver can efficiently test for an error by checking this bit first. This bit is read only. Standard Host Driver Requirements To simplify error check sequence, the Standard Host Driver should be implemented as follows: In SD mode, the Standard Host Driver sets 0 to the *UHS-II Error Interrupt Status Enable* register so that the driver may check the *Error Interrupt Status* register alone when this status (**Error Interrupt**) is set to 1. In UHS-II mode, the Standard Host Driver sets 0 to the *Error Interrupt Status Enable* register so that the driver may check the *UHS-II Error Interrupt Status* register alone when this status (**Error Interrupt**) is set to 1. 1 Error 0 No Error
14	Rsvd	**Reserved**
13	ROC	**FX Event** This status is added from Version 4.10. Bit06 of response data will be stored in the R[14] of the *Response* register. This interrupt may be used with response check function. In this case, this status is set when R[14] of *Response* register is set to 1 and **Response Type R1 / R5** is set to 0 in the T*ransfer Mode* register or *UHS-II Transfer Mode* register. If response check is disabled, this status is set when R[14] of *Response* register is set to 1. Host Driver needs to screen **FX Event** interrupt by checking response type is R1. 1 FX_EVENT is detected 0 No Event
12	ROC	**Re-Tuning Event (UHS-I only)**

<table>
<tr><td>04</td><td>RW1C</td><td>Buffer Write Ready
This status is set if the Buffer Write Enable changes from 0 to 1. Refer to the Buffer Write Enable in the Present State register.
In UHS-II mode, this bit is set at FC (Flow Control) unit basis.

<table><tr><td>1</td><td>Ready to write buffer</td></tr><tr><td>0</td><td>Not ready to write buffer</td></tr></table></td></tr>
<tr><td>03</td><td>RW1C</td><td>DMA Interrupt
This status is set if the Host Controller detects the SDMA buffer boundary during transfer. Refer to the SDMA Buffer Boundary in the Block Size register.
Other DMA interrupt factors may be added in the future.
In case of ADMA, by setting Int field in the descriptor table, Host Controller generates this interrupt. Suppose that it is used for debugging.
This interrupt shall not be generated after the Transfer Complete.

<table><tr><td>1</td><td>DMA Interrupt is generated</td></tr><tr><td>0</td><td>No DMA Interrupt</td></tr></table></td></tr>
<tr><td>02</td><td>RW1C</td><td>Block Gap Event
This status is checked with generation of Transfer Complete interrupt by setting the Stop At Block Gap Request in the Block Gap Control register. Host determines whether the transaction is completed or can continue:
=1: The transaction is stopped on the way and can be restarted by using Continue Request in the Block Gap Control register
=0: The transaction is already completed and host is not required to set Continue Request

Timing of this status on non-DMA data transfer
(1) In the case of non-DMA Read Transaction
This bit is set at the falling edge of the DAT Line Active Status (When the transaction is stopped at SD Bus timing. The Read Wait shall be supported in order to use this function. Refer to Section 3.12.3 about the detail timing.
(2) In the case of non-DMA Write Transaction
This bit is set at the falling edge of Write Transfer Active Status (After getting CRC status at SD Bus timing). Refer to Section 3.12.4 for more details on the sequence of events.

Timing of this status on DMA data transfer
This status shall be valid by generating Transfer Complete and the timing depends on bus timing and DMA implementation.

<table><tr><td>1</td><td>Transaction stopped at block gap (not completed)</td></tr><tr><td>0</td><td>No Block Gap Event</td></tr></table></td></tr>
<tr><td>01</td><td>RW1C</td><td>Transfer Complete
This bit indicates stop of transaction on three cases:
(1) Completion of data transfer
(2) Completion of a command pairing with response-with-busy (R1b, R5b)
(3) Stop of data transfer by setting Stop At Block Gap Request in the Block Gap Control register</td></tr>
</table>

Following explanation about the timing of generating this status is for the case of non-DMA operations. SD Bus transaction timing (busy or data block) determines the timing of this status. In case of DMA operation, timing of this status depends on DMA implementation.

(1) SD Mode

(a) In the case of a Read Transaction
This bit is set at the falling edge of **Read Transfer Active Status**. This interrupt is generated in two cases. The first is when a data transfer is completed as specified by data length (After the last data has been read to the Host System). The second is when data transfer has stopped at the block gap by setting the **Stop At Block Gap Request** in the *Block Gap Control* register. Refer to Section 3.12.3 for more details as an example of non-DMA.

(b) In the case of a Write Transaction
This bit is set at the falling edge of the **DAT Line Active Status**. This interrupt is generated in two cases. The first is when the last data is written to the SD card as specified by data length and the busy signal released. The second is when data transfers are stopped at the block gap by setting **Stop At Block Gap Request**. Refer to Section 3.12.4 for more details as an example of non-DMA.

(c) In the case of a command pairing with response-with-busy
This bit is set when busy is de-asserted. Refer to **DAT Line Active** and **Command Inhibit (DAT)** in the *Present State* register.

(d) In UHS-I mode
While performing tuning procedure (**Execute Tuning** is set to 1), **Transfer Complete** is not set to 1**.**

(2) **UHS-II Mode**
This interrupt is generated in following two cases:

(a) EBSY Completion (for EBSY supported commands)
When **EBSY Wait** in the *UHS-II Transfer Mode* register is set to 1, this bit is set when EBSY packet has been received, and all valid data have been sent to system memory in case of read operation.

(b) Stop/Continue during DCMD Data Transfer
When **Stop At Block Gap Request** in the *Block Gap Control* register is set to 1 and data transfer is stopped at the Flow Control.

Following is for both SD mode and UHS-II mode.
The table below shows that **Transfer Complete** has higher priority than **Data Timeout Error**. If both bits are set to 1 together, suppose execution of a command is completed.

Relation between Transfer Complete and Data Timeout Error

Transfer Complete	Data Timeout Error	Meaning of the status
0	0	Interrupted by another factor
0	1	Timeout occur during transfer
1	Don't Care	Command Execution complete

1	Command execution is completed
0	Not complete

<table>
<tr>
<td>00</td>
<td>RW1C</td>
<td>
Command Complete
(1) SD Mode
This bit is set when get the end bit of a response except the case of Auto CMD12 and Auto CMD23. Command Complete is not generated by the response of CMD12 or CMD23 but generated by the response of a read/write command.
Refer to Command Inhibit (CMD) in the Present State register for how to control this bit.

The table below shows that Command Timeout Error has higher priority than Command Complete. If both bits are set to 1, it can be considered that the response was not received correctly.

<table>
<tr><th>Command Complete</th><th>Command Timeout Error</th><th>Meaning of the status</th></tr>
<tr><td>0</td><td>0</td><td>Interrupted by another factor</td></tr>
<tr><td>Don't Care</td><td>1</td><td>Response not received within 64 SDCLK cycles.</td></tr>
<tr><td>1</td><td>0</td><td>Response received</td></tr>
</table>

Version 4.00 defines response check function for R1 and R5. If Response Interrupt Disable in the Transfer Mode register is set to 1, generation of this interrupt is prohibited regardless of Command Complete Signal Enable.

(2) UHS-II Mode
If Response Interrupt Disable is set to 0 in the UHS-II Transfer Mode register, this interrupt is generated when response packet is received.
If Response Interrupt Disable is set to 1 in the UHS-II Transfer Mode register, generation of this interrupt is prohibited regardless of Command Complete Signal Enable.

<table>
<tr><td>1</td><td>Command complete</td></tr>
<tr><td>0</td><td>No command complete</td></tr>
</table>
</td>
</tr>
</table>

Table 2-24 : Normal Interrupt Status Register