OSI Week06a

Physical Memory Protection (PMP)

(a) pmpaddr[0-63]

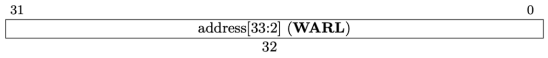

Figure 3.33: PMP address register format, RV32.

(b) pmpcfg[0-15]

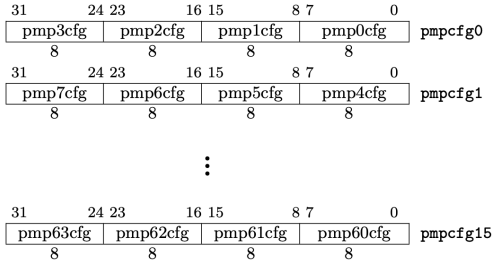

Figure 3.31: RV32 PMP configuration CSR layout.

(c) pmp[0-63]cfg

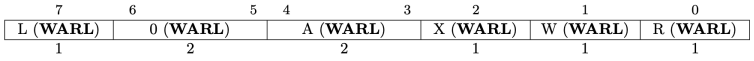

Figure 3.35: PMP configuration register format.

(d) pmp[0-63]cfg.A

A	Name	Description
0	OFF	Null region (disabled)
1	TOR	Top of range
2	NA4	Naturally aligned four-byte region
3	NAPOT	Naturally aligned power-of-two region, ≥8 bytes

Table 3.10: Encoding of A field in PMP configuration registers.