OSI Week8a

1.SDMA workflow

Start

(1) Set System Address Reg.

(2) Set Block Size Reg.

(3) Set Block Count Reg.

(4) Set Argument Reg.

(5) Set Transfer Mode Reg.

(6) Set Command Reg.

(7) Wait for Command Complete Int.

Command Complete Int. occur

(8) Clear Command Complete status

(9) Get Response Data
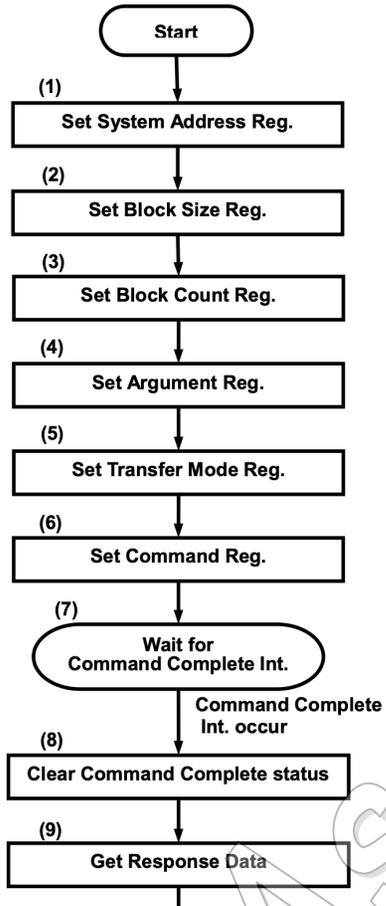
2.SD Host Control Register Map

Offset	15-08 bit	07-00 bit	Offset	15-08 bit	07-00 bit
002h	SDMA System Address (High)		000h	SDMA System Address (Low)	
006h	16-bit Block Count		004h	Block Size	
00Ah	Argument (High)		008h	Argument (Low)	
00Eh	Command		00Ch	Transfer Mode	
012h	Response1		010h	Response0	
016h	Response3		014h	Response2	
01Ah	Response5		018h	Response4	
01Eh	Response7		01Ch	Response6	
022h	Buffer Data Port1		020h	Buffer Data Port0	
026h	Present State		024h	Present State	
02Ah	Wakeup Control	Block Gap Control	028h	Power Control	Host Control 1
02Eh	Software Reset	Timeout Control	02Ch	Clock Control	
032h	Error Interrupt Status		030h	Normal Interrupt Status	
036h	Error Interrupt Status Enable		034h	Normal Interrupt Status Enable	

3. Commands

Command Index	Argument	Response	Description
CMD12	None(0)	R1b	Stop to read data.
CMD17	Address[31:0]	R1	Read a block.
CMD18	Address[31:0]	R1	Read multiple blocks.
CMD24	Address[31:0]	R1	Write a block.
CMD25	Address[31:0]	R1	Write multiple blocks.