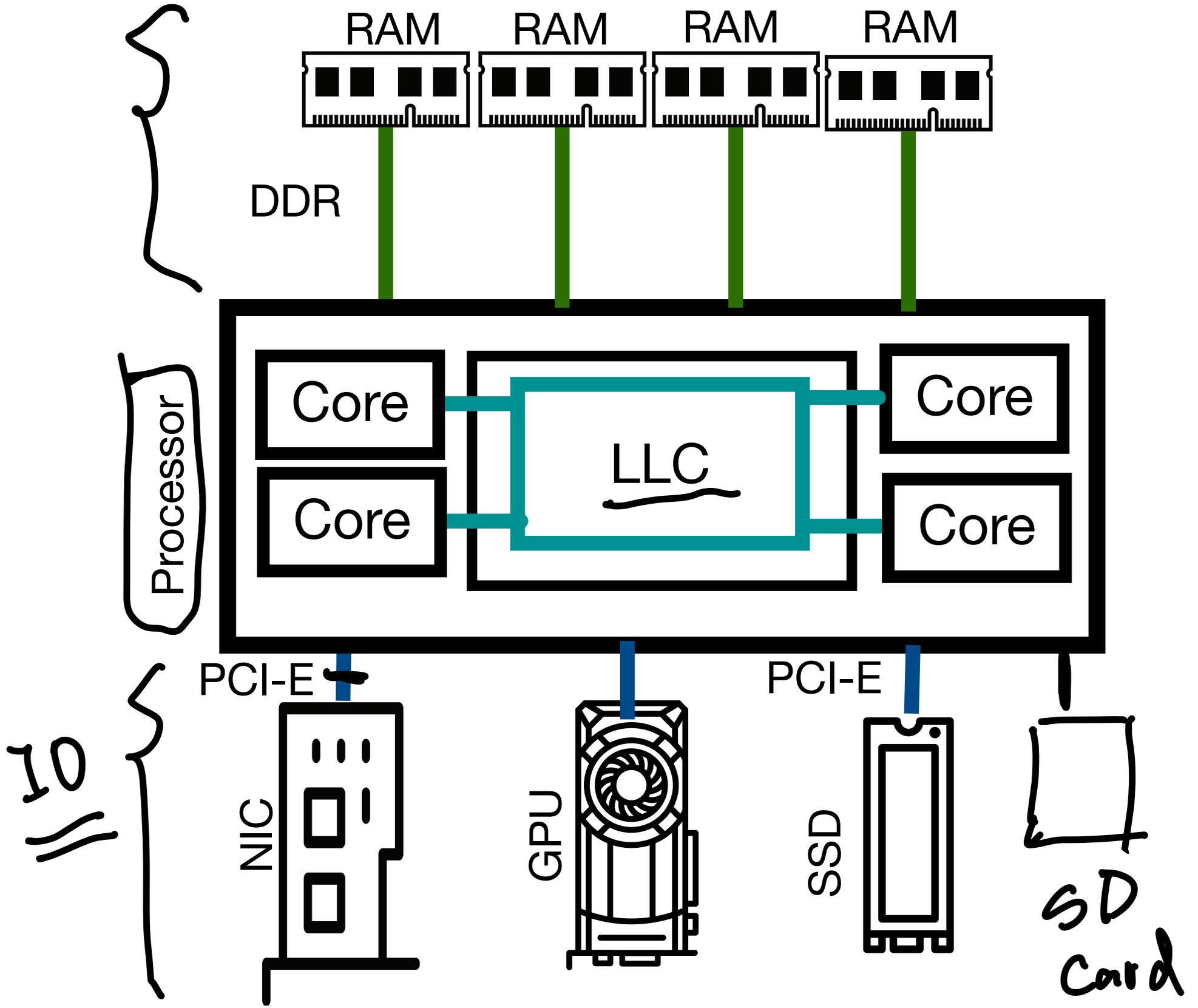
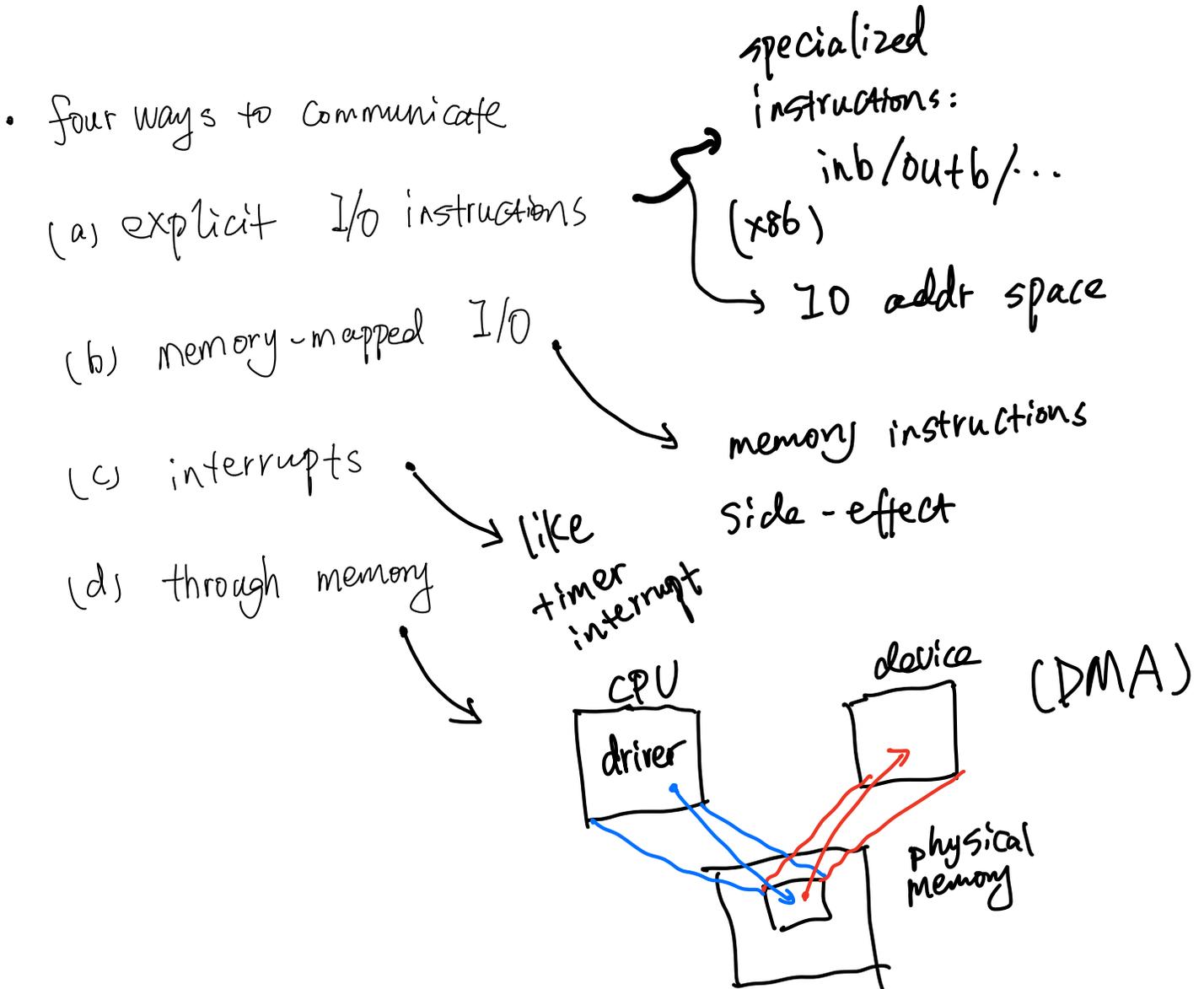


# Machine



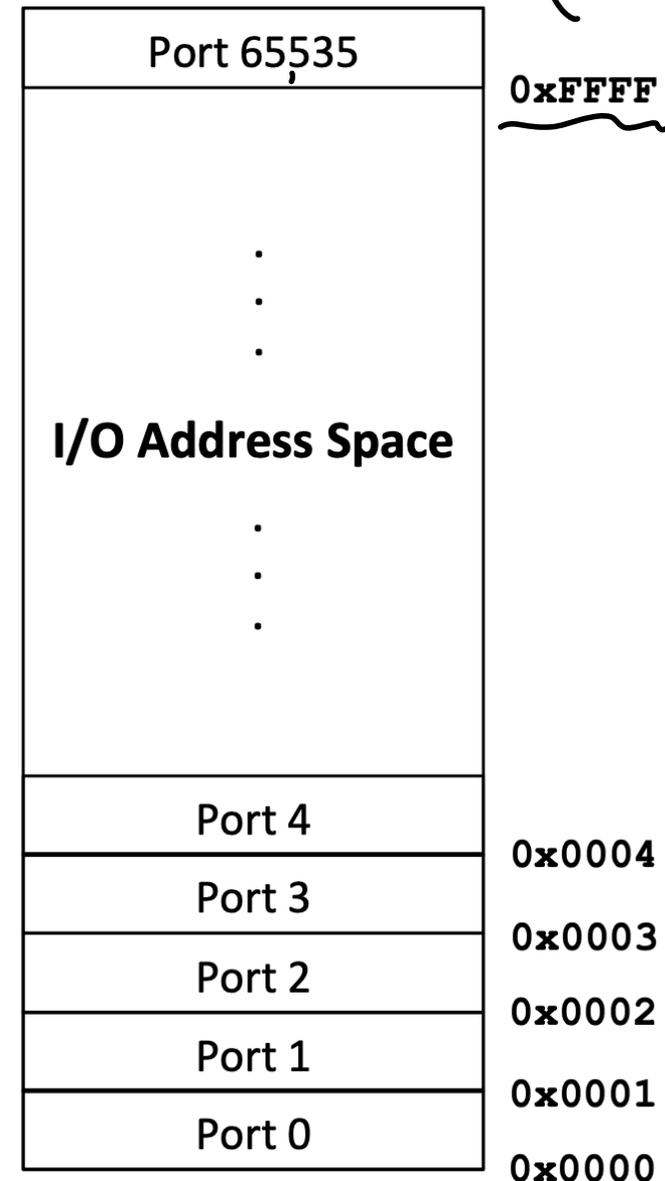
- ✓ 0. Recap: four ways of communication
  - ✓ 1. An example: a tty dev
  - ✓ 2. Communication configurations
  - ✓ 3. Hints about Lab6 (SD card driver)
- 

• logistics

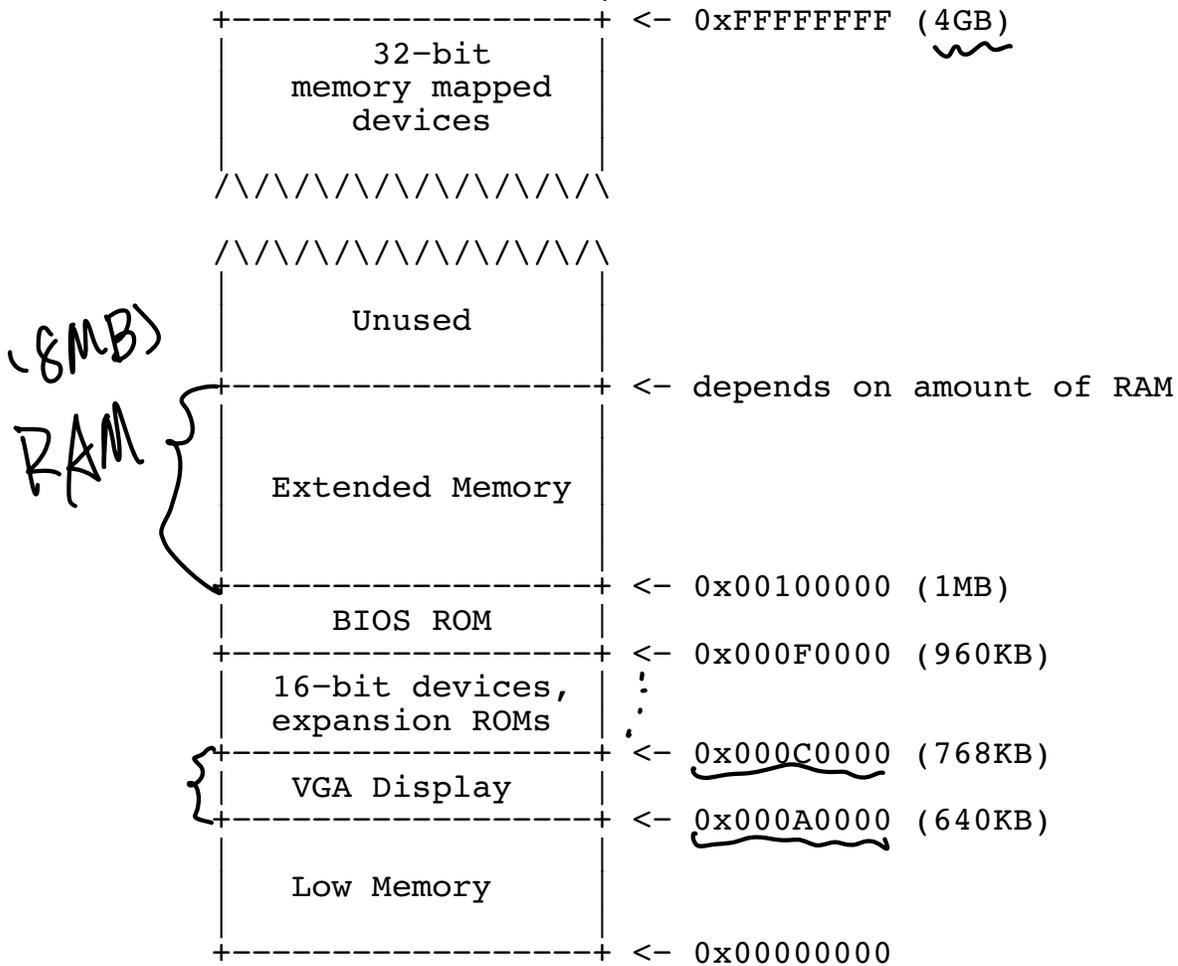


# Port I/O Address Space

- Software and hardware architectures of x86 architecture support a separate address space called "I/O Address Space"
  - Separate from memory space
- ① Access to this separate I/O space is handled through a set of I/O instructions
  - IN, OUT, INS, OUTS
- Access requires Ring0 privileges
  - Access requirement does not apply to all operating modes (like Real-Mode)
- The processor allows 64 KB+3 bytes to be addressed within the I/O space
- Harkens back to a time when memory was not so plentiful
- You may never see port I/O when analyzing high-level applications, but in systems programming (and especially BIOS) you will see lots of port I/O
- One of the biggest impediments to understanding what's going on in a BIOS



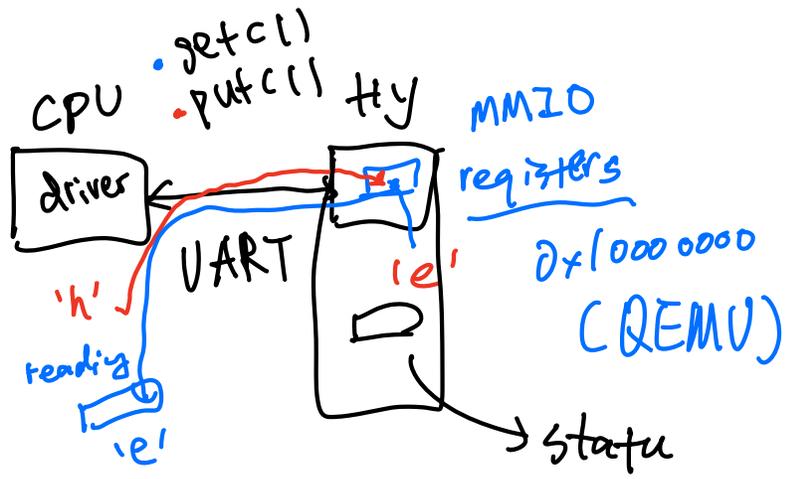
\* Here is a 32-bit PC's physical memory map:



[Credit to Frans Kaashoek, Robert Morris, and Nickolai Zeldovich for this picture]

1. An example: UART and a tty device

Spec  
Demo



2. Communication configurations

- A. Polling vs. interrupts
  - B. DMA vs. programmed I/O
- ① status of devices
- ② transfer data

polling: `while ( ... );` ← status ← // CPU core

interrupt

prog I/O

`for ( ... ) {`  
`register = c;`  
`}` ← MMIO ← // CPU core

receive livelock

DMA

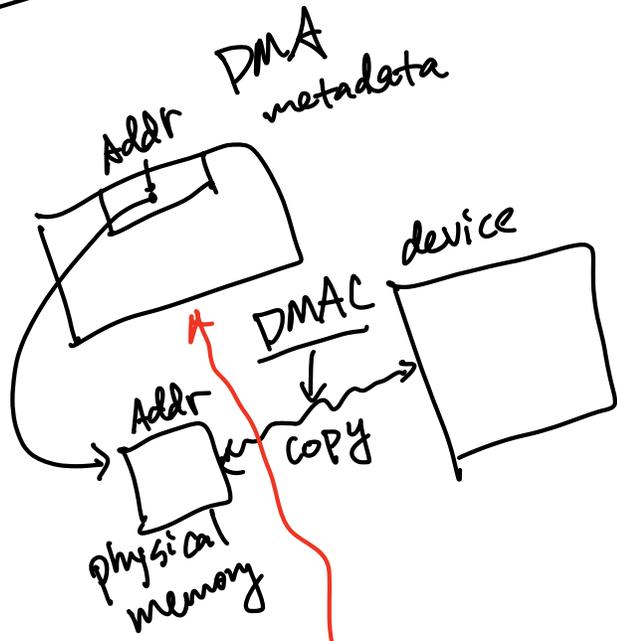
prog I/O

interrupt

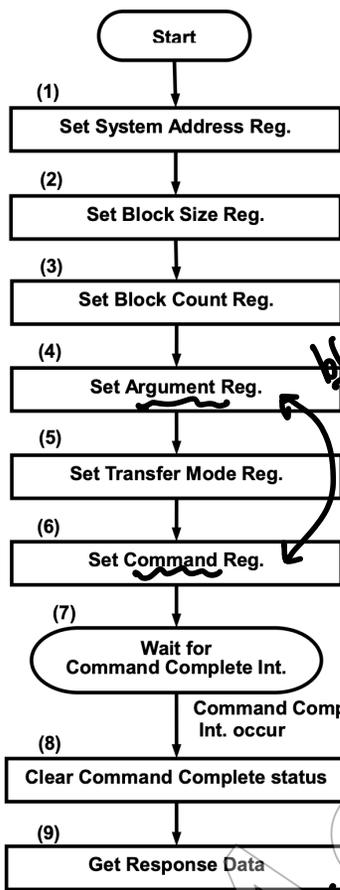
polling

SD Card

tty

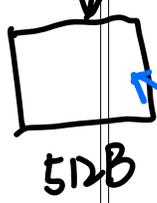


1. SDMA workflow



• read <sup>one</sup> block from SD card

block no \* BLOCK\_SIZE  
↳ LBA



polling

Any errors?

2. SD Host Control Register Map

Offset	15-08 bit	07-00 bit	Offset	15-08 bit	07-00 bit
002h	SDMA System Address (High)		000h	SDMA System Address (Low)	
006h	16-bit Block Count		004h	Block Size 512B	
00Ah	Argument (High)		008h	Argument (Low)	
00Eh	Command		00Ch	Transfer Mode	
012h	Response1		010h	Response0	
016h	Response3		014h	Response2	
01Ah	Response5		018h	Response4	
01Eh	Response7		01Ch	Response6	
022h	Buffer Data Port1		020h	Buffer Data Port0	
026h	Present State		024h	Present State	
02Ah	Wakeup Control	Block Gap Control	028h	Power Control	Host Control 1
02Eh	Software Reset	Timeout Control	02Ch	Clock Control	
032h	Error Interrupt Status		030h	Normal Interrupt Status	
036h	Error Interrupt Status Enable		034h	Normal Interrupt Status Enable	

BASE



3. Commands

Command Index	Argument	Response	Description
CMD12	None(0)	R1b	Stop to read data.
CMD17	Address[31:0]	R1	Read a block.
CMD18	Address[31:0]	R1	Read multiple blocks.
CMD24	Address[31:0]	R1	Write a block.
CMD25	Address[31:0]	R1	Write multiple blocks.

