

Interrupts and Control Status Registers (CSRs)

[borrowed from Yunhao's
CS 4411/5411: Practicum in Operating Systems, 22fall]

The mtvec CSR



Value	Name	Description
0	Direct	All exceptions set pc to BASE.
1	Vectored	Asynchronous interrupts set pc to BASE+4×cause.
≥2	—	Reserved

Table 3.5: Encoding of mtvec MODE field.

The *mstatus* CSR

31	30																	23	22	21	20	19	18	17
SD	WPRI								TSR	TW	TVM	MXR	SUM	MPRV										
1	8								1	1	1	1	1	1										
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0								
XS[1:0]	FS[1:0]	MPP[1:0]	WPRI	SPP	MPIE	WPRI	SPIE	UPIE	MIE	WPRI	SIE	UIE												
2	2	2	2	1	1	1	1	1	1	1	1	1												

MIE stands for machine interrupt enable

RISC-V privileged spec

The **mie** CSR (not mstatus.MIE)

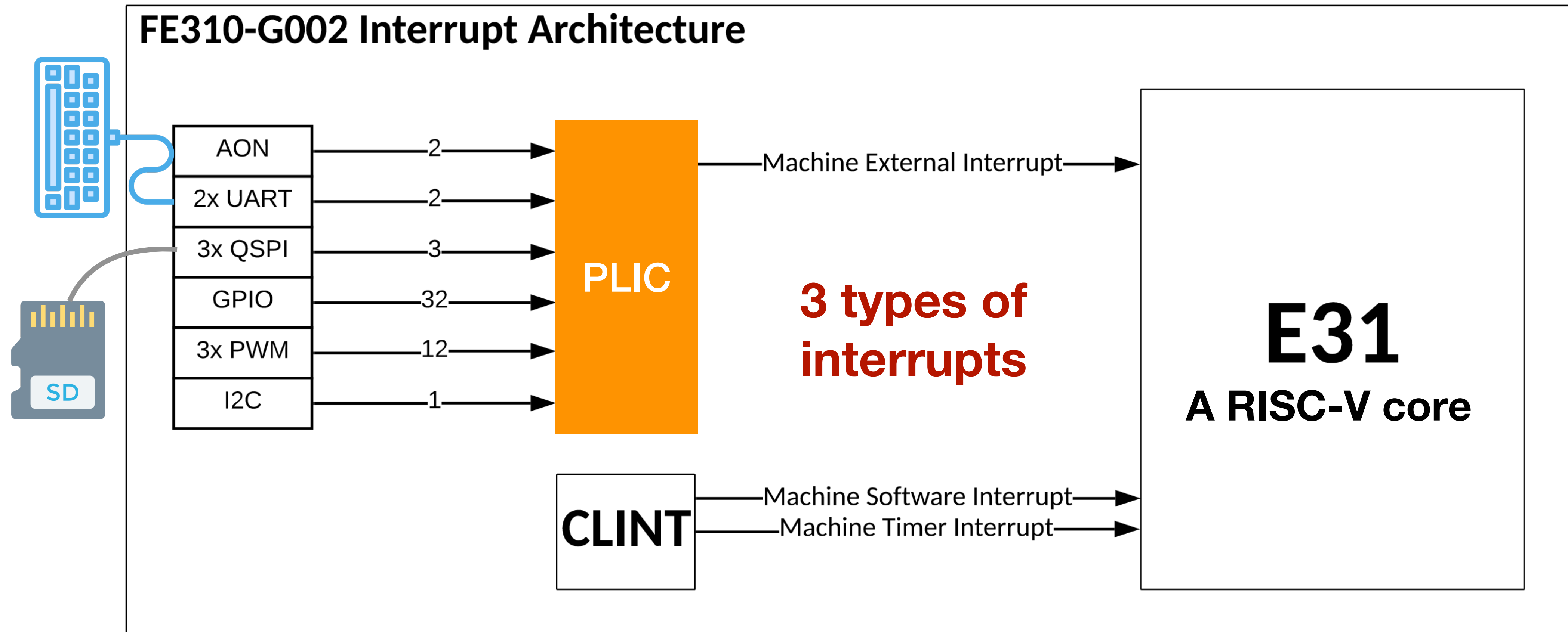
XLEN-1	12	11	10	9	8	7	6	5	4	3	2	1	0
WPRI	MEIE	WPRI	SEIE	UEIE	MTIE	WPRI	STIE	UTIE	MSIE	WPRI	SSIE	USIE	
XLEN-12	1	1	1	1	1	1	1	1	1	1	1	1	

MTIE stands for machine timer interrupt enable

Next...

- interrupts beyond CLINT (e.g., timer interrupts)
- RISC-V fine-grained control of interrupts
- how to know which interrupt is triggered?

Platform Interrupt Controller (**PLIC**)



`mie` provides fine-grained control

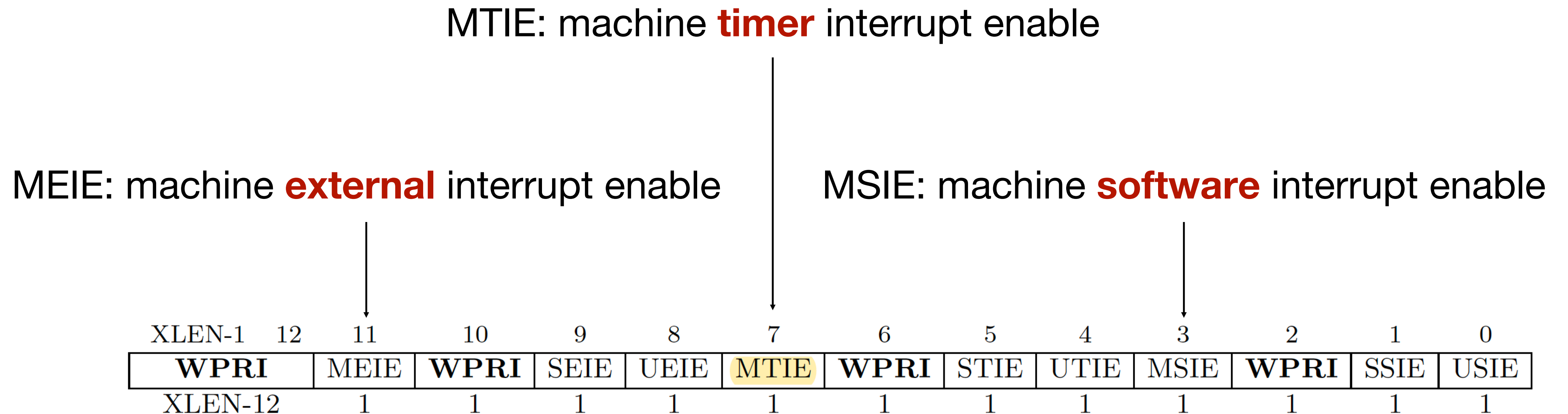


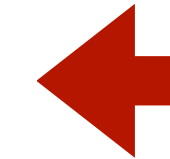
Figure 3.12: Machine interrupt-enable register (`mie`).

Timer is interrupt #7

Interrupts

Exceptions

Interrupt	Exception Code	Description
1	0	<i>Reserved</i>
1	1	Supervisor software interrupt
1	2	<i>Reserved</i>
1	3	Machine software interrupt
1	4	<i>Reserved</i>
1	5	Supervisor timer interrupt
1	6	<i>Reserved</i>
1	7	Machine timer interrupt
1	8	<i>Reserved</i>
1	9	Supervisor external interrupt
1	10	<i>Reserved</i>
1	11	Machine external interrupt
1	12–15	<i>Reserved</i>
1	≥16	<i>Designated for platform use</i>
0	0	Instruction address misaligned
0	1	Instruction access fault
0	2	Illegal instruction
0	3	Breakpoint
0	4	Load address misaligned
0	5	Load access fault
0	6	Store/AMO address misaligned
0	7	Store/AMO access fault
0	8	Environment call from U-mode
0	9	Environment call from S-mode
0	10	<i>Reserved</i>
0	11	Environment call from M-mode
0	12	Instruction page fault
0	13	Load page fault
0	14	<i>Reserved</i>
0	15	Store/AMO page fault
0	16–23	<i>Reserved</i>
0	24–31	<i>Designated for custom use</i>
0	32–47	<i>Reserved</i>
0	48–63	<i>Designated for custom use</i>
0	≥64	<i>Reserved</i>



System calls?

Interrupts

Exceptions

Interrupt	Exception Code	Description
1	0	<i>Reserved</i>
1	1	Supervisor software interrupt
1	2	<i>Reserved</i>
1	3	Machine software interrupt
1	4	<i>Reserved</i>
1	5	Supervisor timer interrupt
1	6	<i>Reserved</i>
1	7	Machine timer interrupt
1	8	<i>Reserved</i>
1	9	Supervisor external interrupt
1	10	<i>Reserved</i>
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0	6	Store/AMO address misaligned
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0	10	<i>Reserved</i>
0	11	Environment call from M-mode
0	12	Instruction page fault
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